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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,244	08/18/2003	Sheng-Chih Lai	0941-0809P	8162

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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,244	LAI ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *12-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed May 12, 2005 have been fully considered but they are not persuasive.

2. Applicants contend that Johnson , U.S. Patent 6,525,953 B1 herein known as Johnson fails to teach or suggest any dielectric layer formed directly on any diodes.

3. In response to Applicants contention that Johnson fails to teach or suggest any dielectric layer formed directly on any diodes, please see column 1, lines 24-26 where Johnson clearly discloses dielectric formed on the diodes (also see column 1, lines 47-60).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson, U.S. Patent 6,525,953 B1.

6. Johnson discloses a semiconductor device as claimed. See **FIGS. 1-17**, where Johnson teaches the claimed invention.

7. Pertaining to claim 1, Johnson teaches a mask read only memory containing diodes, comprising:

a semiconductor substrate **100**;

an insulating layer **102** on the semiconductor substrate;

a plurality of first conductive lines **114** along a first direction on the insulating layer;

a plurality of vertical diodes **12** on the first conductive lines;

a plurality of dielectric layers **120** on part of the diodes; and

a plurality of second conductive lines **123/128** along a second direction on the dielectric layers and the diodes, wherein the first direction is perpendicular to the second direction.

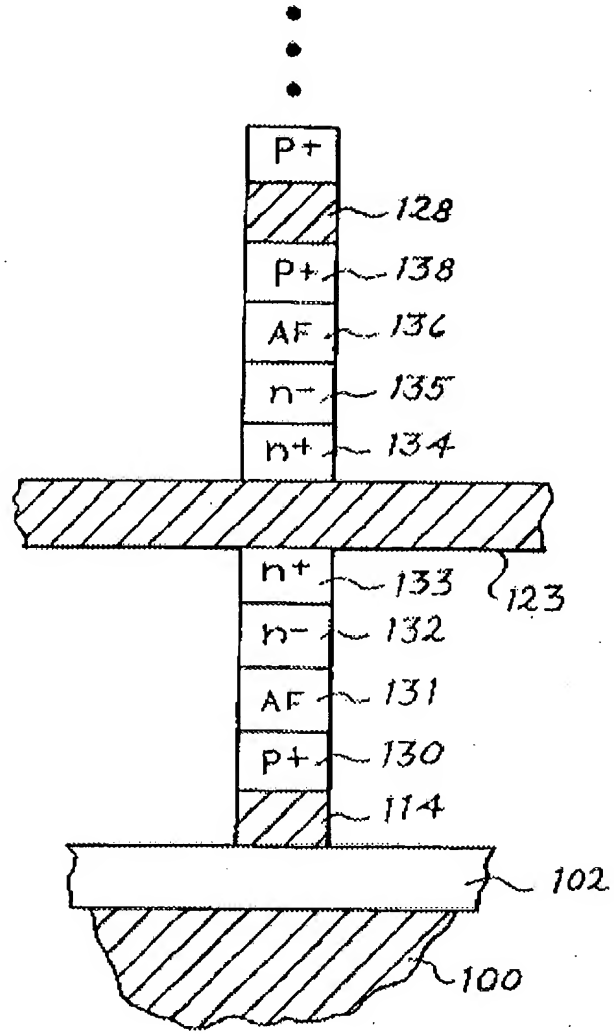


Fig. 7

8. Pertaining to claim 2, Johnson teaches the mask read only memory containing diodes as claimed in claim 1, wherein the diodes are PN diodes.

9. Pertaining to claim 3, Johnson teaches the mask read only memory containing diodes as claimed in claim 2, wherein the PN diodes comprise two polysilicon layers of opposing conductive types.

10. Pertaining to claim 4, Johnson teaches the mask read only memory containing diodes as claimed in claim 1, wherein the insulating layer is silicon dioxide, aluminum oxide (Al_2O_3), silicon nitride (Si_3N_4), tantalum pentoxide (Ta_2O_5) , barium strontium titanate (BST), hafnium oxide (HfO_2), or titanium dioxide (TiO_2) .

11. Pertaining to claim 5, Johnson teaches the mask read only memory containing diodes as claimed in claim 1, wherein the first conductive lines are bit lines and the second conductive lines are word lines (column 4, lines 60-63).

12. Pertaining to claim 6, Johnson teaches the mask read only memory containing diodes as claimed in claim 1, wherein the dielectric layers are silicon dioxide, aluminum oxide (Al_2O_3), silicon nitride (Si_3N_4) , tantalum pentoxide (Ta_2O_5) , barium strontium titanate (BST), hafnium oxide (HfO_2), or titanium dioxide (TiO_2) .

13. Pertaining to claim 7, Johnson teaches the mask read only memory containing diodes as claimed in claim 1, comprising: a semiconductor substrate;

an insulating layer on the semiconductor substrate; and

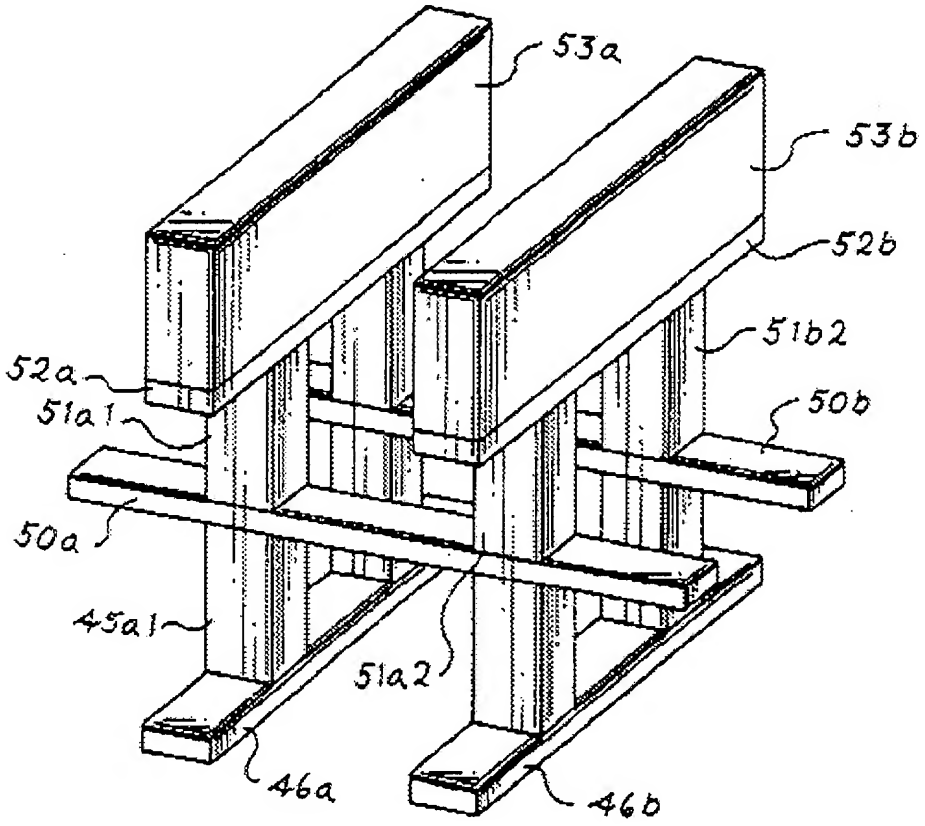
at least two memory cell layers stacked on the insulating layer wherein there is a separating layer between any two memory cell layers to provide insulation and wherein each memory cell layer comprises:

a plurality of first conductive lines along a first direction on the insulating layer;

a plurality of vertical diodes on the first conductive lines; a plurality of dielectric layers on part of the diodes; and a plurality of second conductive lines along a second direction on the dielectric layers and the diodes, wherein the first direction is perpendicular to the second

direction, wherein any two adjacent upper and lower diode layers are disposed opposite to one another so that two sides thereof of opposing conductive type face each other.

Fig. 10(f)



14. Pertaining to claim 8, Johnson teaches the mask read only memory containing diodes as claimed in claim 7, which comprises 2 to 10 memory cell layers.

15. Pertaining to claim 9, Johnson teaches the mask read only memory containing diodes as claimed in claim 7, wherein the separating layer is silicon dioxide, aluminum oxide ($A1_2O_3$), silicon nitride (Si_3N_4) , tantalum pentoxide (Ta_2O_5), barium strontium titanate (BST), hafnium oxide (HfO_2), or titanium dioxide (TiO_2) .

16. Pertaining to claim 10, Johnson teaches the mask read only memory containing diodes as claimed in claim 1, comprising:

a semiconductor substrate;

an insulating layer on the semiconductor substrate;

n diode layers stacked on the insulating layer, wherein n is an integer equal to or greater than 2 and each diode layer comprises a plurality of vertical diodes and a plurality of dielectric layers on part of the diodes; and

(n + 1) parallel conductive layers disposed between the bottom diode layer and the insulating layer, on the top diode layer, and between any

two adjacent diode layers respectively, wherein the (n + 1) parallel conductive layers are disposed so that any two adjacent conductive layers are perpendicular to each other, wherein any two adjacent upper and lower diode layers are disposed opposite to one another so that two sides of matching conductive type face each other (also see column 7, lines 35-53).

17. Pertaining to claim11, Johnson teaches the mask read only memory containing diodes as claimed in claim 10, wherein n is between 2 and 10.

18. Pertaining to claim 20, Johnson teaches a mask read only memory containing diodes, comprising:

a semiconductor substrate;

an insulting layer on the semiconductor substrate;

a plurality of first conductive lines along a first direction on the insulating layer;

first and second vertical diodes on the first conductive lines;

a plurality of dielectric layers directly on the diodes (the Examiner takes the position that the phrase "subsequent dielectric depositions" is plural meaning more than one); and

a plurality of second conductive lines along a second direction directly on the dielectric layers and the second vertical diodes, wherein the first direction is perpendicular to the second direction.

19. Claims 1-11 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Shingu Masataka Japanese Patent Applicant Publication Abstract 06-334139

Conclusion

20. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on July 11, 2005 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

21. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8100.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC